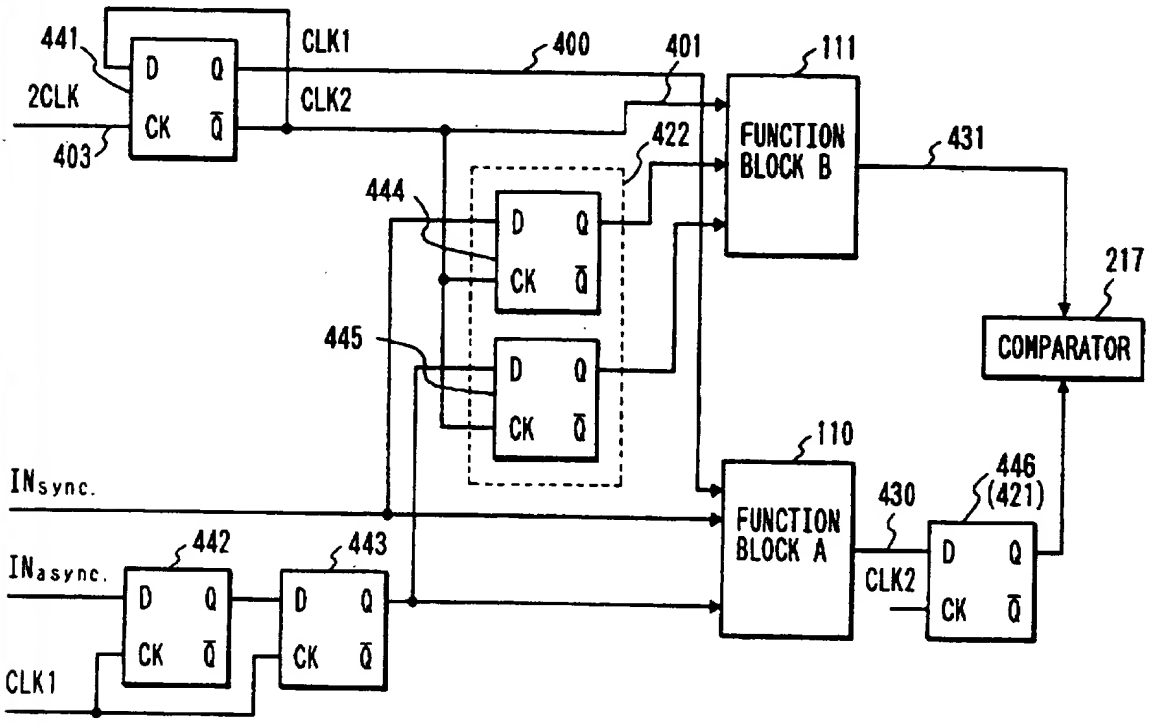
## REMARKS/ARGUMENTS

In the current Office Action, which is dated May 2, 2005, at page 2, in paragraph 5, the Examiner objected to the specification, requiring the abstract to be provided on a separate page. Accordingly, attached hereto is a separate page containing the abstract.

In paragraph 7 at the bottom of page 2 of the current Office Action, the Examiner rejected Claim 8 for anticipation by US Patent 5,802,266 granted to Kanekawa et al. The Examiner merely repeated Applicant's claim language as recited in Claim 8 followed by the citation "(fig. 49, abstract, col. 27, line 58-col. 28, line 4, col. 28, lines 8-12, Kanekawa et al.)." However, the Examiner did not provide a one-to-one correspondence between the limitations in Claim 8 and the corresponding features in Kanekawa's FIG. 49. This defect in the current Office Action has made it difficult to respond to the anticipation rejection, although a response is attempted in good faith, as follows.

Specifically, Kanekawa's FIG. 49, which is cited against Claim 8, is reproduced below for convenience.




It is unclear, from the Office Action, whether the Examiner believes that Claim 8's "combinatory logic circuit" limitation is met by Kanekawa's function block A 110 or by Kanekawa's function block B 111, or by some combination of elements in this figure.

SILICON VALLEY
ATENT GROUP LLP
0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

Moreover, Claim 8 requires two flip-flops which are driven by the same clock, wherein a first flip-flop receives the output of the combinatory logic circuit and a second flip-flop receives the same output delayed by a predetermined duration. It is unclear, from the Office Action, as to which one of the six flip-flops 441-446 in the above figure is being analogized to Claim 8's "first flip-flop" and which one of the remaining five flip-flops in the above figure is being analogized to Claim 8's "second flip-flop".

Also, it is unclear, from the Office Action, whether the Examiner contends that Kanekawa's comparator 217 is being analogized to Claim 8's "analysis circuit." Even assuming that comparator 217 is the claimed "analysis circuit," note that comparator 217 is coupled to the output of only one flip-flop, namely flip-flop 446. Comparator 217 is further coupled to function block B 111 (which as noted above may be analogized to Claim 8's "combinatory logic circuit"). Hence, comparator 217 is not coupled to the outputs of the two flip-flops as required by Claim 8.

Finally, note that coupling of an analysis circuit to two flip-flops wherein one flip-flop receives a delayed version of the signal received by the other flip-flop, as recited in Claim 8, is nowhere disclosed or suggested by Kanekawa's patent.

In view of the above-discussed remarks, Applicant respectfully requests the Examiner to withdraw the rejection of Claim 8 over the teachings of Kanekawa's patent. If the Examiner continues to reject Claim 8 in the next Office Action, Applicant requests the Examiner to provide a one-to-one correspondence between each claim limitation and the corresponding feature in the cited prior art reference. Also, if the Examiner continues to reject Claim 8 over the teachings of Kanekawa, then the next Office Action must be made non-final due to the above-noted defects in the rejection in the current Office Action.

Note that Claim 8 is amended to eliminate the word "synchronization" in reference to the "first flip-flop" because this limitation is not required in view of the prior art of record. Moreover, Claim 8 is re-written to clarify the language in conformance with the US practice, without narrowing the scope of protection being sought. Specifically, "a combinatory logic circuit having at least one output connected to a first flip-flop" has been rewritten for clarity into two separate limitations as follows. The first limitation requires a combinatory logic circuit having at least one output, while the second limitation requires the first flip-flop to be connected to receive said output. Moreover, the reference numerals

SILICON VALLEY
ATENT GROUP LLP
0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

previously recited in Claim 8 have now been eliminated, in conformance with the US practice. Finally, the last limitation in Claim 8 is now changed to explicitly state a previously-inherent limitation therein, namely that the analysis circuit is coupled to receive the outputs of the first flip-flop and the second flip-flop (with an error being indicated if different). Hence, Applicant respectfully requests the Examiner to approve these changes to Claim 8.

Also, a newly added Claim 11, which depends from Claim 8, is believed to be patentable for at least the same reason as Claim 8. For an illustrative embodiment of Claim 11, see Applicant's FIG. 8A and also the related description at page 14 line 19 to page 15 line 29.

Claim 1 was rejected in the current Office Action, in paragraph 10 at pages 3 and 4, over the teachings of Helm (US Patent 5,072,450) as modified by the teachings of Byers (US Patent 5,416,362). Neither of these two references discloses or suggests a circuit that is protected, as recited in the preamble of Claim 1.

Specifically, Applicant respectfully traverses the Examiner's statement (at line 3 in paragraph 10) that "Helm et al. teach a circuit protected against transient disturbances..." This statement by the Examiner is completely baseless, i.e. unsupported in the citation given by the Examiner, namely "(figure 1, col. 3, lines 20-33)". Specifically, nothing in Helm's figure 1 indicates that Helm's circuit is protected against transient disturbances. Moreover, in col. 3, lines 20-33 (which are reproduced below for convenience), Helm merely indicates that his circuit detects and indicates the presence of an error:

> The local memory 16 includes a conventional parity check circuit 13 which, as a data word is read from the memory 16 and sent to the CPU 12, generates one or more parity bits for the word and compares them to the parity bits stored with the word. The parity bits generated by the circuit 37 are normally identical to the stored parity bits, and the parity check circuit 37 thus normally outputs a logic low voltage on its output line 38 to indicate that no error has been detected. On the other hand, if the parity bits generated by the circuit 37 are different from the stored parity bits, then an error

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

> has occurred and the circuit 37 produces a logic high voltage on its output line 38 to indicate the presence of an error.

As seen from the above-quoted text, Helm is silent as to what is to be done when an error is indicated. Hence Helm says nothing about how to protect in the presence of error.

In contrast, Claim 1's memory element is controlled, by Claim 1's error control code generation circuit, to keep the memory element's state unchanged when error is present (when the control code is incorrect), and otherwise the memory element is transparent.

Furthermore, note that although Helm uses the same word "transient" as in Claim 1, his usage of this word is limited to transient "errors" as described further at Helm's column 1, lines 38-48 (reproduced below):

> Transient errors, on the other hand, are errors which are marginal, and may come and go. They may, for example, occur only when certain specific patterns of data are stored in the memory. Transient errors frequently are not picked up by the tests which the computer does when it is turned on, and thus the portions of memory having these transient problems may be utilized by the computer with no notice that errors may occur. Of course, the parity detection schemes discussed above are usually capable of detecting the transient error when it occurs.

As seen from the above-quoted text, Helm's transient errors appear to be reproducible, e.g. Helm's error may be repeatedly obtained each time a specific sequence of actions are performed, e.g. if specific patterns of data are stored in memory. This interpretation is supported by Helm's specification at column 7, lines 15-37, wherein Helm describes disabling or replacing the memory module or chip in which the error is found. Hence, Helm's transient error is not a "disturbance", as described in Applicant's original specification, at for example, page 1, lines 1-3. Helm is silent on how to overcome "disturbances" of the type recited in Claim 1, i.e. how to form a protected circuit which can withstand such disturbances. A skilled artisan would not look to Helm's parity detection

SILICON VALLEY
ATENT GROUP LLP
0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

circuitry, when faced with the problem of creating a circuit that is protected against external "disturbances", for example from heavy ion bombardments. Applicant submits that Helm's patent is non-analogous art, i.e. not from the same field as the current patent application. Hence, Helm is being inappropriately applied in rejecting Claim 1.

Applicant further submits that Byers fails to overcome the above-noted defects in the teachings of Helm.

Also, the Examiner failed to provide any prior art citation for a motivation or suggestion to add Byers transparent flip-flop to the parity detection circuit taught by Helm.

The Examiner further failed to identify how the combination of Byers's flip-flop is to be made with Helm's circuitry. In particular, Byers discloses a flip-flop having nine input lines 21-29 (see Fig. 1; and column 2, lines 62-63). The Examiner has not indicated in the Office Action, as to which of these nine inputs of Byers' flip-flop is to be connected to which of the outputs in Helm's circuitry. Hence, it is unclear as to what particular combination is being applied against Claim 1.

If this rejection is continued in the next Office Action, the Examiner must identify the specific connections between each of the nine inputs of Byers' flip-flop to corresponding nine outputs of Helm's circuitry. Moreover, the Examiner must identify a motivation or suggestion in the prior art which supports the specific combination being proposed by the Examiner (as opposed to other combinations).

Moreover, even assuming that the Examiner is successful in forming a working combination of Byers' flip-flop with Helm's circuitry, Applicant respectfully submits that the combination does not teach the invention recited in Claim 1 for at least the following additional reason. Byers merely discloses a transparent flip-flop wherein the input data flows through to the output when the transparency line is enabled, and the transparent flip-flop returns to latching (i.e. the incoming data is latched) when the line is disabled. See Byers' column 1, line 64 to column 2, line 2 (which is the same text that the Examiner cited for rejecting Claim 1).

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

In contrast, Claim 1's memory element is transparent when there is no error, and keeps it's output's state unchanged when the error control code is incorrect. Neither of the two references being cited against Claim 1 discloses or suggests this type of memory element.

Hence Claim 1 is believed to be patentable for one or more of the reasons discussed above. Note that Claim 1 has been re-written to more explicitly state this limitation, which was previously inherent therein, and hence there is no change in scope.

If the Examiner continues to reject Claim 1 over the teachings of Helm and Byers, then the next Office Action must be made non-final due to the above-noted defects in the rejection of Claim 1 in the current Office Action.

Claim 6 was rejected in paragraph 13 on page 6 of the current Office Action, for being obvious in view of the teachings of Oprescu (US Patent 5,467,464) as modified by the teachings of Kanekawa (US Patent 5,802,266). Applicant respectfully traverses this rejection as being an un-supported combination of Examiner-selected features from the prior art references. Specifically, Oprescu teaches how to re-synchronize signals Rx Clock and Rx Data, by sending signal Rx Clock (see line 102 in FIG. 5) through successive delay elements 108, and comparing the delayed signals with Rx Data (on line 104) in flip-flops 110. There is no reason why a skilled artisan, when faced with the problem of creating a circuit that is protected against external disturbances, would look to Oprescu's synchronizing circuitry. The Examiner has failed to indicate why synchronization is necessary to protect against external disturbances. Applicant further submits that Oprescu's patent is non-analogous art, i.e. not from the same field as the current patent application. Hence, Oprescu is being inappropriately applied in rejecting Claim 6.

The Examiner further failed to identify how Oprescu's synchronizing circuitry is to be modified by Kanekawa's comparator. In fact the Examiner failed to identify any figure number and any reference number e.g. to explicitly identify Kanekawa's comparator to be added to Oprescu's synchronizing circuitry. Even assuming the Examiner is referring to Kanekawa's comparator 217 in FIG. 49, it is unclear as to which two flip-flops in Oprescu's synchronizing circuitry are to have their outputs compared? Furthermore, nothing in Kanekawa's patent even remotely suggests using his comparator with successive delay elements. Moreover, Applicant submits that use of successive delay elements would not work in the device of Kanekawa.

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

Also, the Examiner failed to provide any prior art citation for a motivation or suggestion to add Kanekawa's comparator to the chain of delay elements taught by Oprescu.

Therefore, Claim 6 is patentable for one or more of the reasons discussed above. Note that Claim 6 has been re-written to more explicitly state this limitation, which was previously inherent therein, and hence there is no change in scope.

Claim 9 was rejected in paragraph 15 on page 7 of the current Office Action, for being obvious in view of the teachings of O'Lear (US Patent 3,904,891) as modified by the teachings of Byers (US Patent 5,416,362) and Stewart (US Patent 4,464,754). Once again, Applicant respectfully traverses this rejection as being an un-supported combination of Examiner-selected features from the prior art references. Specifically, O'Lear teaches a circuit for selectively transferring the true or complement data bit from one register to another register (see column 6 at lines 7-12 and 49-55). O'Lear's disclosure is silent on what happens in case of a transient disturbance. In fact there is no indication whatsoever by O'Lear of any kind of fault or disturbance. Therefore, the Examiner's statement that O'Lear teaches a circuit protected against transient disturbances (see 3rd line in paragraph 15 on page 7 of the current Office Action) is without basis.

While O'Lear does disclose multiple identical circuits (see fig. 2 and column 7, lines 28-39), note that these circuits merely represent multiple bit slices of a multibit design. O'Lear's circuits are not redundant, because if a disturbance happens, then an error will occur. The Examiner has failed to indicate why a skilled artisan would be motivated to re-wire the multiple identical circuits to operate redundantly with one another to provide protection from disturbances.

Furthermore, in modifying O'Lear's circuit by use of Byers' teachings the Examiner merely stated "Byers et al. in an analogous art teach that the present invention ... latched through the system (col. 1, line 64-col. 2, line 2, Byers et al)" (see top of page 8 of the current Office Action). Applicant submits that Byers' teachings are defective, for the reasons noted above in reference to Claim 1. Specifically, Byers fails to overcome the defects in the teachings of O'Lear. Moreover, the Examiner failed to provide any prior art citation for a motivation or suggestion to add Byers' transparent flip-flop to O'Lear's circuit for transferring selectively true/complement bits.

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

The Examiner further failed to identify how the nine input lines 21-29 of Byers's flip-flop are to be coupled to O'Lear's circuitry. Specifically, the Examiner has not indicated in the Office Action, as to which of these nine inputs of Byers' flip-flop is to be connected to

which of the outputs in O'Lear's circuitry. Hence, it is unclear as to what particular combination is being applied against Claim 9.

If this rejection is continued in the next Office Action, the Examiner must identify the specific connections between each of the nine inputs of Byers' flip-flop to corresponding nine outputs of O'Lear's circuitry. Moreover, the Examiner must identify a motivation or suggestion in the prior art which supports the specific combination being proposed by the Examiner (as opposed to other combinations).

Moreover, as noted above, Byers merely discloses a transparent flip-flop, wherein the input data flows through to the output when the transparency line is enabled, and alternatively returns to latching when the line is disabled. None of the references being cited against Claim 9 discloses or suggests a memory element that is transparent when its two inputs are identical, and that keeps its state unchanged when the two inputs are different.

Therefore, Claim 9 is patentable for one or more of the reasons discussed above. Note that Claim 9 has been re-written to more explicitly state the limitation discussed in the previous paragraph, which limitation was previously inherent therein, and hence there is no change in scope.

Moreover, Applicant respectfully traverses the rejections of all dependent claims for at least the reasons described above for their respective independent claims. Regarding the dependent claims as well, Applicant respectfully submits that the Office Action fails to explicitly identify specific connections between the features being combined, and further fails to provide a prior art reference that suggests or motivates the combination being proposed by the Examiner.

Hence, Applicant respectfully requests allowance of all pending claims. If there are any questions please call the undersigned at (408) 982-8203.

**Via Express Mail Label No.**
**EV 581 855 805 US**

Respectfully submitted,

S. Omkar

Omkar K. Suryadevara
Attorney for Applicant & Assignee
Reg. No. 36,320

SILICON VALLEY
ATENT GROUP LLP

0 Mission College Blvd
Suite 360
anta Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210